Features

- 3.3V voltage supply;
- Supports 8X28G electrical interface;
- Loops back TX to RX on all 8 ports;
- I2C interface & MSA compatible & Custom memory maps;
- 5 independent power heathers, with 0.2W solution up to 15W;
- 4 Thermistors on PCBA (Optional two on the shell) ;
- Hot pluggable module;
- 2 statues LED indicator;
- Temperature monitor and alarms warning;
- Low speed signal control;
- Voltage monitoring;
- Insertion counter;
- Visual software interface for power setting, temperature display and temperature alarm

Operating Conditions

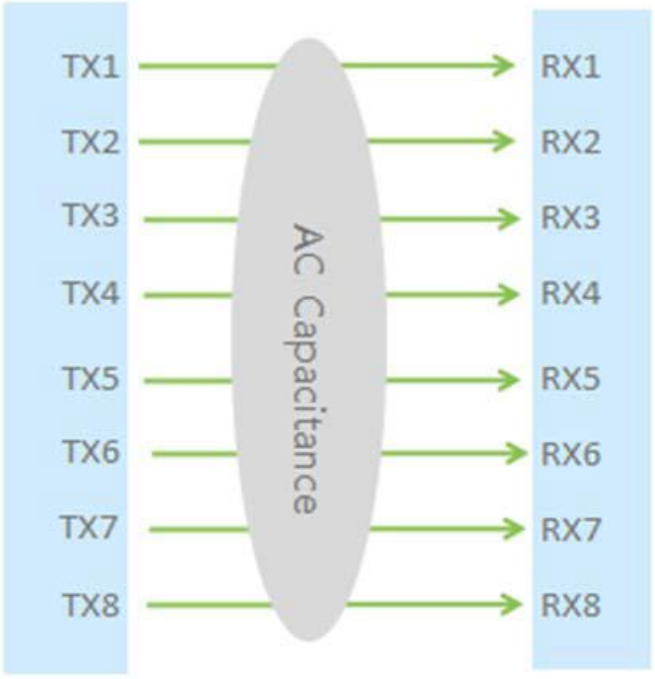
Parameter	*Symbol*	*Conditions*	*Min.*	*Typ.*	*Max.*	*Units*
Operating Temperature	*TA*		0		115	°C
Supply Voltage	V_{cc}		3.0	3.3	3.6	V
Data Rate	*Rb*	Guaranteed to work at 28Gbps per lane (support PAM4)	0		200 & 400	Gbps
Input/ Output Load Resistance	*Impedance*	AC-Coupled, Differential	85	100	110	ohm
Power Class		Programmable to Emulate 1-8 power classes	0		15	W

High Speed Signals

High speed signals are electrically lopped back from TX side to RX side of the module; all differential TX pairs are connected to the corresponding RX pairs.

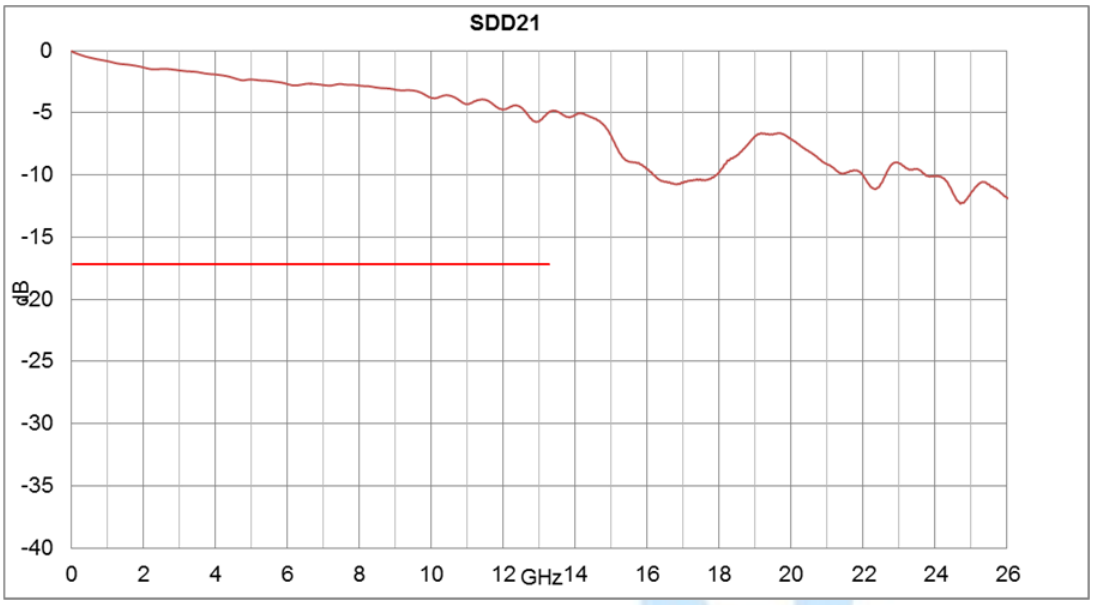
The Passive traces connecting TX to RX pairs are designed to support a data rate up to 28Gbps.

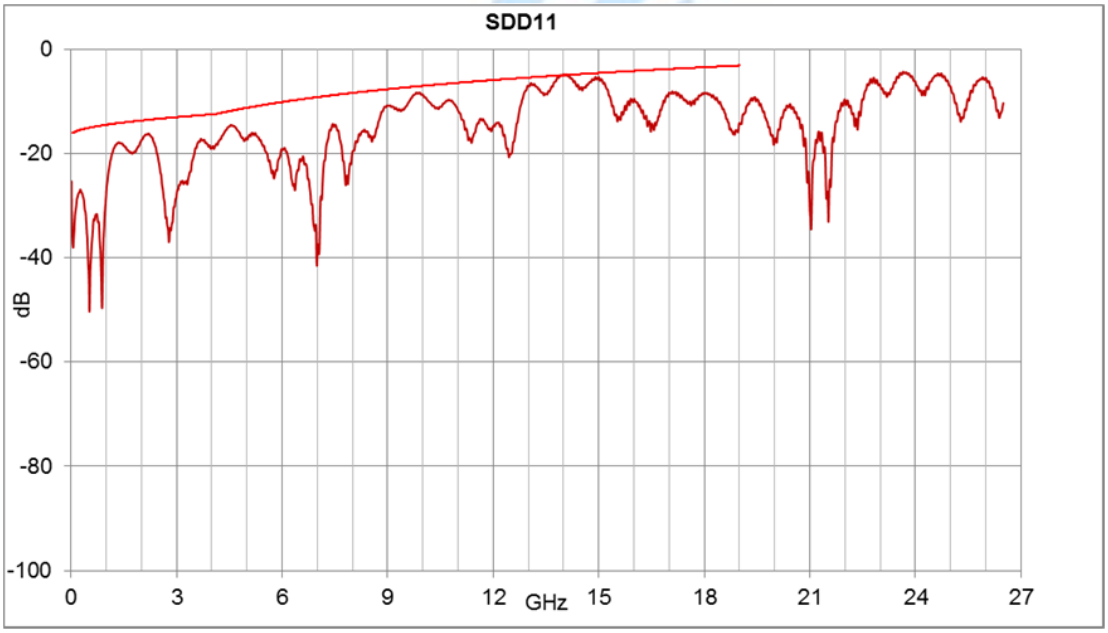
a) Function



b) IL and RL graphs

The test is performed in accordance with IEEE802.3cd.

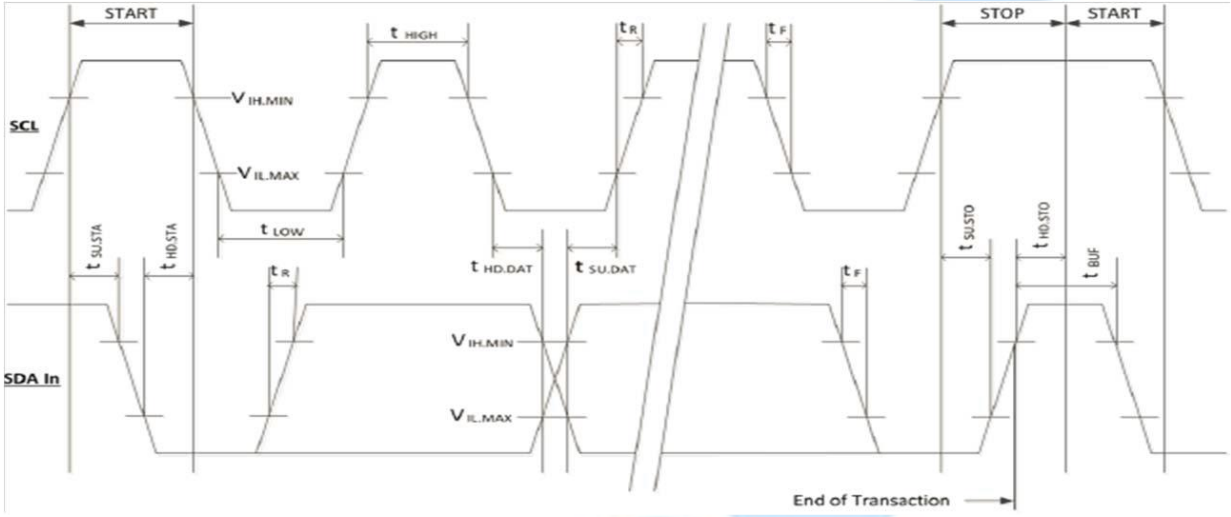




I2C communication interface

The Module supports the I2C interface. This QSFP-DD specification is based on the QSFP-DD Hardware and closely follows the QSFP SFF-8636 specification.

Timing Diagram:



		Fast Mode (400 KHz)		Fast Mode Plus (1 MHz)			
Parameter	Symbol	Min	Max	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	400	0	1000	KHz	
Clock Pulse Width Low	tLOW	1.3		0.50		µs	
Clock Pulse Width High	tHIGH	0.6		0.26		µs	
Time bus free before new transmission can start	tBUF	20		1		µs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		0.26		µs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.6		0.26		µs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		0		µs	
Data In Setup Time	tSU.DAT	0.1		0.1		µs	
Input Rise Time	tR		300		120	ns	From (VIL,MAX=0.3*Vcc) to (VIH, MIN=0.7*Vcc)
Input Fall Time	tF		300		120	ns	From (VIH,MIN=0.7*Vcc) to (VIL,MAX=0.3*Vcc)
STOP Setup Time	tSU.STO	0.6		0.26		µs	
STOP Hold Time	tHD.STO	0.6		0.26		us	

LED indicator

Add plug-in two-color LED lights at the rear of the PCB, extending outside the shell. It is used for power consumption and other indications of module operation only.

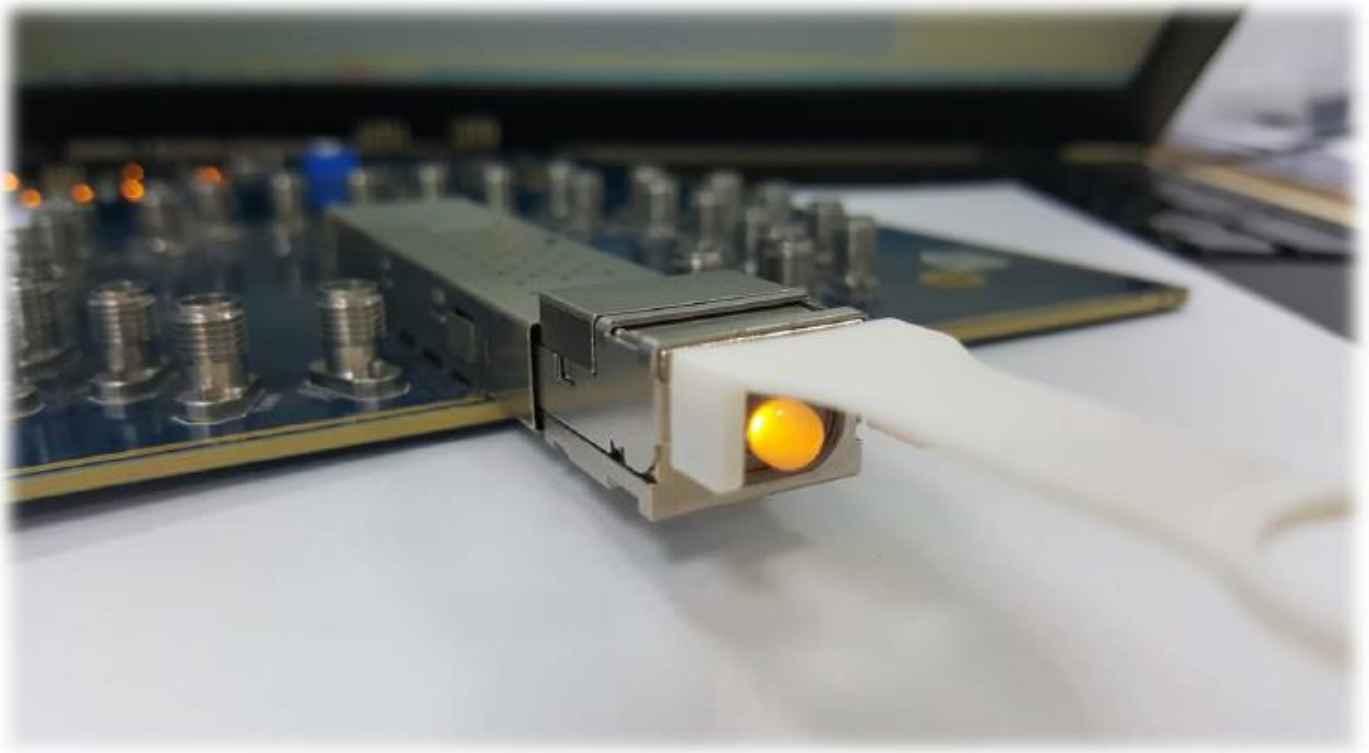
Green-Signifies that the module is working in normal mode (high power mode);

Orange-Signifies that the module is working in unnormal mode or low power mode;

Green (Blinking)-Signifies that the module is work in normal mode and I2C communication disable;

Orange (Blinking)-Signifies that the module is work in unnormal mode and I2C communication disable.

Plug-in two-color LED:



Power control

A total of 5 power thermal modules are designed for this module, and the EEPROM Map 132-135 bit is used for PWM data storage controlled by IIC. In high power mode, the power will change with the register value. In low power mode，PWM turns off.

There are four 4W and one 3W power modules, the power range is 0-15W and the resolution is 0.2W.

Device address: 0xA0

Page	Address	Bit	Name	Description
Page3(RW)	131	7-0	PWM1	PWM Control 0-3W
	132	7-0	PWM2	PWM Control 0-4W
	133	7-0	PWM3	PWM Control 0-4W
	134	7-0	PWM4	PWM Control 0-4W
	135	7-0	PWM5	PWM Control 0-4W

Temperature sensors & Cut-off

A total of 4 temperature sensors are designed in the module, 2 temperature chips adopts IIC mode and 2 SMD NTC adopts IIC mode to measure PCBA temperature, 2 welded NTC reserved can be fixed on the shell to detect the temperature(optional).

The value read by the temperature sensor is stored in the corresponding register of Memory Maps. In order to avoid the module overheating, the fixed temperature is set in the corresponding register. Once overheating, the PWM will be turned off. If it is lower than the critical value, PWM returns to the previous value.

To avoid overheating the module, a Cut-off temperature is pre-defined. The module is continuously monitoring the temperature and checking its value against the Cut-Off temperature. Once the module temperature reaches the cut-off temperature, the PWM will automatically turn off in order to prevent overheating. Once the temperature is 5 degrees below cut-off value, the PWM goes back to its previous value. The Warning temperature for the module is 100℃. The Cut-off temperature for the module is 115℃.

Device address: 0XA0

Page	Address	Bit	Name	Description
Page0(R)	14-15	7-0	Temperature1	Maximum temperature measured on PCBA
Page3(R)	138-139	7-0	Temperature2	Maximum temperature measured on PCBA
	140-141	7-0	Temperature3	Maximum temperature measured on PCBA
	142-143	7-0	Temperature4	Maximum temperature measured on PCBA
Page3(R/W)	136	7-0	Cut off Temperature	Cut off Temperature when module overheating

Insertion counter

The Insertion counter contains the number of times the module was plugged in a host. The insertion counter is incremented every time the module goes in initializing sequence, as it is nonvolatile it is always saved, and can be read anytime from registers 129 and 130 on memory page 3.

Device address: 0xA0

Page	Address	Bit	Name	Description
Page3(RW)	128-129	7-0	Insertion Counter LSB	LSB unit =1 insertion

Voltage monitoring

The MCU on the PCBA module has a voltage detection circuit which can measure the voltage Vcc provided by the internal module. The measurement ranges from 0 to 3600 mV with an accuracy of 0.1 mV.

Device address: 0xA0

Page	Address	Bit	Name	Description
Page0(R)	16-17	7-0	Supply VCC	Modular Power Supply Voltage Measurement

Device information read/write access

Device address: 0xA0

Address	Name	Read	Write
00-13	Module dynamic information	PW0	PW2
18-117	Module dynamic information	PW0	PW2
118-121	Password change Entry	0x00	>PW0
122-125	Password Entry	0x00	PW0
126	Bank select	PW0	PW0
127	Page select	PW0	PW0

Note:

1. PW0: null pass word Access right
2. PW1:0x00 0x00 0x10 0x11
3. PW2:0XA6 0x06 0x4C 0x6E
4. NA: writing invalid, it does not affect the initial value
5. Initial values are fixed values or sequences
6. Passwords need to be entered step by step to open advanced privileges

Device address: 0xA2, register address: 119-127, power off, data auto-clearing.

Low speed signal

a) Modsel

The ModSelL is an input pin. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When the ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host and the LED will be blinking. ModSelL signal input node must be biased to the “High” state in the module.

In this design, the ModseIL is pulled up to Vcc with 5.11k resistor.

b) ResetL

The ResetL pin must be pulled to Vcc in the QSFP-DD module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting “low” an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

In this design, the ResetL is pulled up to Vcc with 5.11k resistor.

c) LPMode

The Module should be in low power mode if the LPMode pin is in the high state, or if the Power_ override bit is in the high state and the Power_set bit is also high. The module should be in high power mode if the LPMode pin is in the low state, or the Power_override bit is high and the Power_set bit is low. Note that the default state for the Power_override bit is low.

In low power mode module will stop all power dissipation and LED changes color to orange, in high power mode the power dissipation will be set to value inside register 98 and LED will be green (normal operation).

In this design, the LPMode is pulled up to Vcc with 5.11k resistor.

d) ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted “Low” when inserted and deasserted “High” when the module is physically absent from the host connector.

In this design, the ModPrsL is pulled to ground with 200Ω resistor.

e) IntL

IntL is an output pin, when “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to host supply voltage on the host board.

In this design, the IntL is pulled up to Vcc with 5.11k resistor.

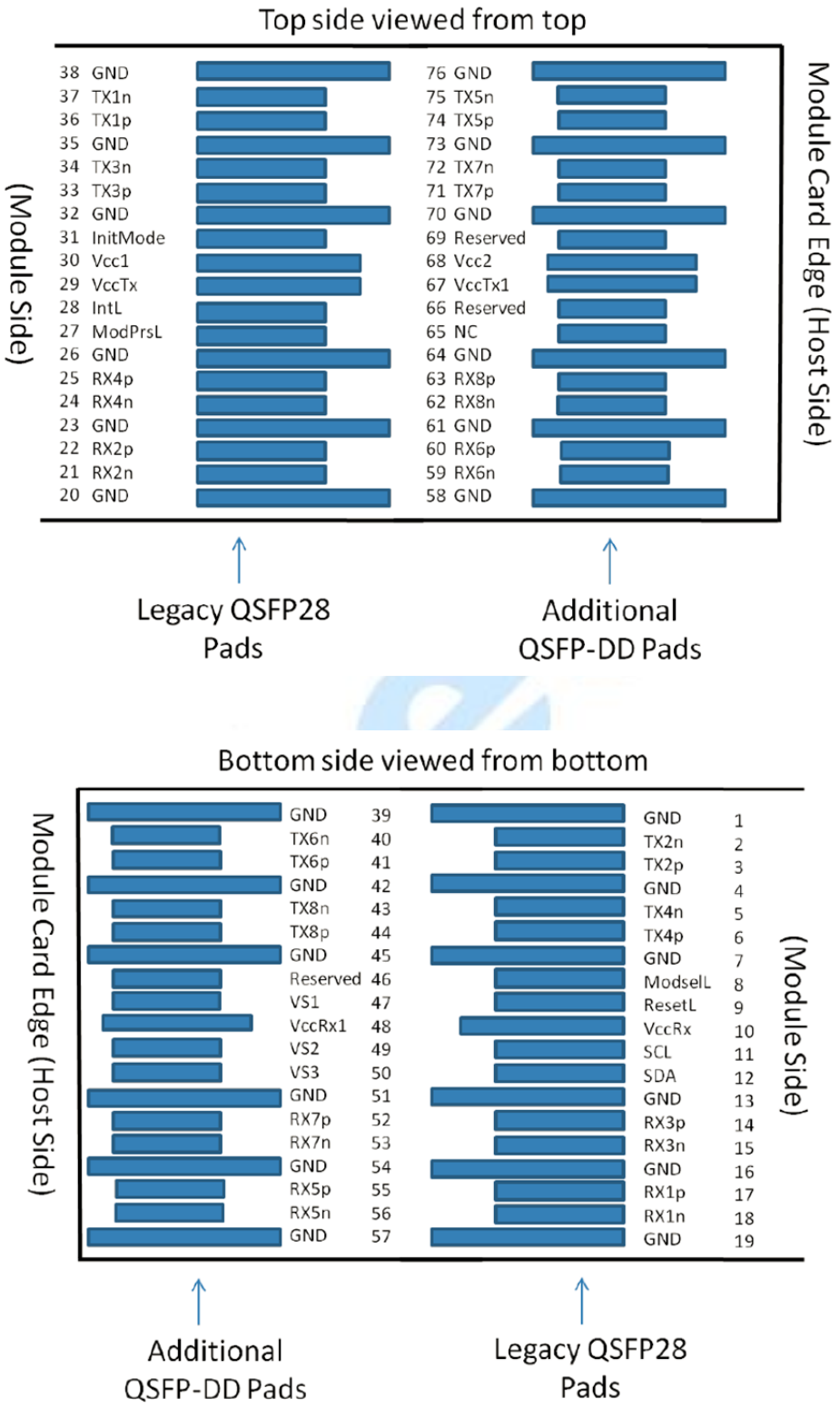
f) SCL&SDA

The corresponding requirements in the agreement are as follows：

SCL is the 2-wire interface clock and SDA is the 2-wire interface data line. SCL and SDA are pulled up to Vcc_Host_2w by resistors in the host.

I2C Read/Write functionality is referred to QSFP-DD Hardware specification.

QSFP-DD Pin define



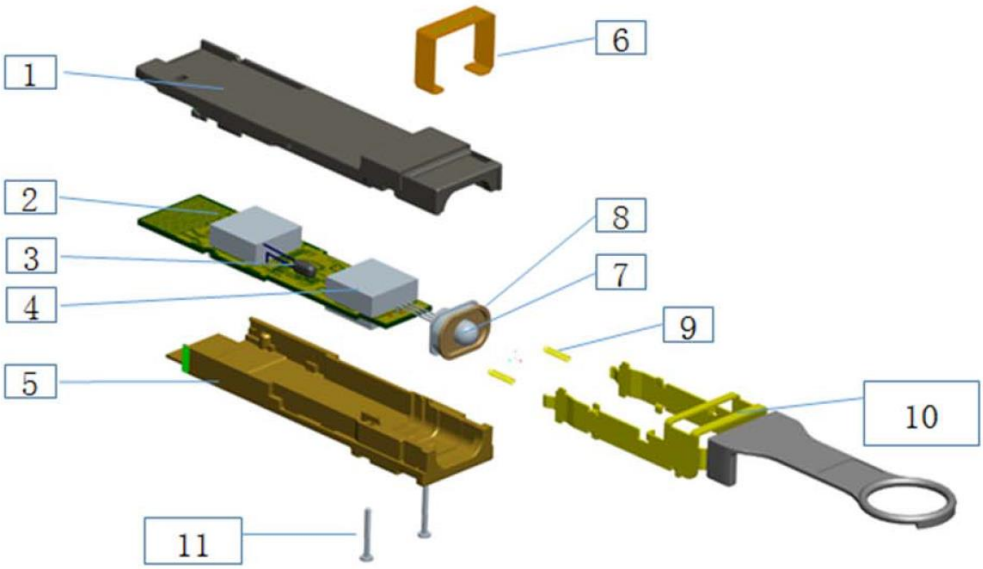
Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

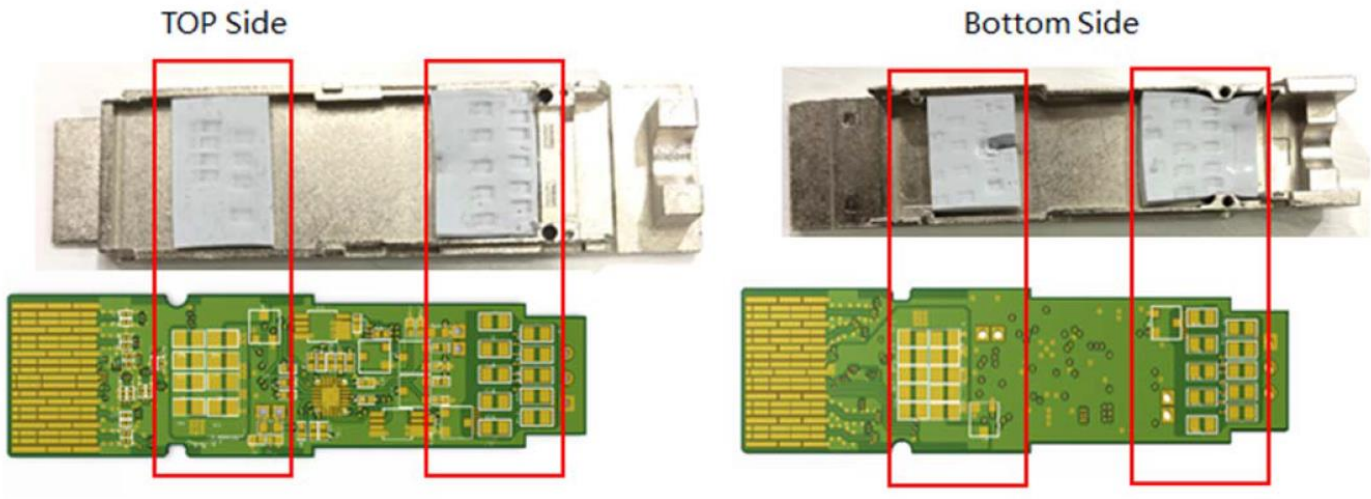
Mechanical design

Explosion Map

1.Upper sheel
2.PCBA
3.Thermistor
4.Thermal conductive silica gel
5.Bottom sheel
6.Latch
7.LED
8.Hardware lamp sets
9.Spring
10.Drawstring
11.Rivet



Heat Dissipation Design



Covering 4 heat sources with heat-dissipating glue, and it touches the shell closely after assembly.

Ordering Information

OP QSDD - T - 00 - P X E

Product Code:
MSAS= Mini-SAS;
MSHD=Mini-SAS HD 6~12G;
SFPP=SFP+ 8~10G;
MSFP=Mini SFP;
XFP=XFP 10G;
CX4=CX4 10G;
QDDR=QDDR 20G;
SF28=SFP28 25G;
QSFP=QSFP 40G;
QFDR=FDR 56G;
QS28=QSFP28 100G;
CXP=CXP 120G;
QS56=QSFP56 200G;
QSDD=QSFP-DD 400G

Transceiver Type:
T=Electrical;
F=Optical;
I=Internal Electrical

Cable Length:
X5=0.5M;
01=1M;
03=3M;
05=5M;
07=7M;
10=10M;
15=15M;
20=20M;
A0=100M
xxxx=Customized Length (Unit: CM)
A5=1.5M (For 25G, 56G & over 100G);
B5=2.5M (For 25G, 56G & over 100G);
C5=3.5M (For 25G, 56G & over 100G)
For Loopback Attenuation:
00=0dB;
0A=1dB;
0B=2dB;
0C=3dB;
0D=4dB;
0E=5dB

P=Passive;
A=Active;

DAC AWG:
A=24;
B=26;
C=28;
E=30;
F=32
X=No Media Type (For Loopback)
AOC OD:
K=3.0 mm
For Loopback Power Consumption:
X=0W;
1=1W;
A=1.5W;
2=2W;
B=2.5W;
3=3W;
C=3.5W
4=4W;
5=5W

For Optech Internal ref.

Note: All information contained in this document is subject to change without notice.